CLAIMS

The following is a detailed listing of all claims that are, or were, in the Application.

1. (Canceled)

2. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

a first transistor having a gate, a source, and a drain, wherein the source of the first transistor is connected to the input terminal;

a second transistor having a gate, a source, and a drain, wherein the gate of the first transistor is connected to the drain and the gate of the second transistor, wherein the source of the second transistor is connected to the output terminal;

a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor;

a first current source connected to the drain of the first transistor; and

a second current source connected to the drain of the second transistor.

3. (Original) The buffer circuit of claim 2 wherein each of the first and second current sources comprises a respective transistor having a gate biased by a first bias signal so that the transistor is providing substantially constant current.

4. (Original) The buffer circuit of claim 3 wherein the transistors of the first and second current sources are matched so that any change in a drain-source voltage for one of

the transistor of the first and second current sources is offset by a corresponding change in a drain-source voltage of the other transistor of the first and second current sources.

5. (Original) The buffer circuit of claim 2 comprising:

a third current source connected to the source of the first transistor; and

a fourth current source connected to the source of the second transistor.

6. (Original) The buffer circuit of claim 5 wherein each of the third and fourth current sources comprises a respective transistor having a gate biased by a second bias signal so that the transistor is in saturation.

7. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

a first transistor having a gate, a source, and a drain, wherein the source of the first transistor is connected to the input terminal;

a second transistor having a gate, a source, and a drain, wherein the gate of the first transistor is connected to the drain and the gate of the second transistor, wherein the source of the second transistor is connected to the output terminal;

a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor;

a fourth transistor having a gate, a source, and a drain, wherein the drain of the fourth transistor is connected to the drain of the first transistor;

a fifth transistor having a gate, a source, and a drain, wherein the drain of the fifth transistor is connected to the drain of the second transistor;

wherein the gates of the fourth and fifth transistors are biased by a first bias signal; and

wherein the fourth and fifth transistors are matched so that the same amount of current flows through each of the fourth and fifth transistors.

8. (Previously presented) The buffer circuit of claim 7 comprising:

a sixth transistor having a gate, a source, and a drain, wherein the drain of the sixth transistor is connected to the source of the first transistor;

a seventh transistor having a gate, a source, and a drain, wherein the drain of the seventh transistor is connected to the source of the second transistor;

wherein the gates of the sixth and seventh transistors are biased by a second bias signal; and

wherein the sixth and seventh transistors are matched so that the same amount of current flows through each of the sixth and seventh transistors.

9. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

a first transistor having a gate, a source, and a drain, wherein the source of the first transistor is connected to the input terminal;

a second transistor having a gate, a source, and a drain, wherein the gate of the first transistor is connected to the drain and the gate of the second transistor, wherein the source of the second transistor is connected to the output terminal;

a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor; and

a capacitor connected to the gate of the third transistor.

10. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

a first transistor and a second transistor, each of the first and second transistors having a gate, a source, and a drain, wherein the source of the first transistor is connected to the input terminal, wherein the gate of the first transistor is connected to the drain and the gate of the second transistor, wherein the source of the second transistor is connected to the output terminal;

a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor;

a fourth transistor and a fifth transistor, each of the fourth and fifth transistors having a gate, a source, and a drain, wherein the drain of the fourth transistor is connected to the drain of the first transistor, wherein the drain of the fifth transistor is connected to the drain of the second transistor, wherein the gates of the fourth and fifth transistors are biased by a first bias signal,

a sixth transistor and a seventh transistor, each of the sixth and seventh transistors having a gate, a source, and a drain, wherein the drain of the sixth transistor is connected to the source of the first transistor, wherein the drain of the seventh transistor is connected to the source of the second transistor, wherein the gates of the sixth and seventh transistors are biased by a second bias signal; and

wherein only the first and third transistors are in active operation.

11. (Original) The buffer circuit of claim 10 wherein the fourth and the fifth transistors provide substantially constant current.

12. (Original) The buffer circuit of claim 10 wherein the sixth and the seventh transistors provide substantially constant current.

13. (Original) The buffer circuit of claim 10 wherein each of the fourth, fifth, sixth, and seventh transistors are providing substantially constant current.

14. (Original) The buffer circuit of claim 10 wherein the fourth and fifth transistors are matched.

15. (Original) The buffer circuit of claim 10 wherein the sixth and seventh transistors are matched.

16. (Original) The buffer circuit of claim 10 comprising a capacitor connected to the gate of the third transistor.

17. (Canceled)

18. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

at most three transistors operable to provide signal currents, wherein two of the three transistors are matched;

wherein the output signal is fed back to the two matched transistors to counter any change in the input signal appearing at the input terminal;

a first current source connected to the one of the two matched transistors; and

a second current source connected to the other of the two matched transistors.

19. (Original) The buffer circuit of claim 18 wherein each of the first and second current sources comprises a respective transistor having a gate biased by a first bias signal so that the transistor is providing substantially constant current.

20. (Original) The buffer circuit of claim 19 wherein the transistors of the first and second current sources are matched so that any change in a drain-source voltage for one of the transistor of the first and second current sources is offset by a corresponding change in a drain-source voltage of the other transistor of the first and second current sources.

21. (Previously presented) A buffer circuit comprising:

an input terminal operable to receive an input signal;

an output terminal at which an output signal for the buffer circuit is provided;

a first transistor having a gate, a source, and a drain, wherein the source of the first transistor is directly connected to the input terminal;

a second transistor having a gate, a source, and a drain, wherein the gate of the first transistor is connected to the drain and the gate of the second transistor;

a third transistor having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor, wherein the source of the third transistor is connected to the output terminal and to the source of the second transistor; and

wherein the output signal is fed back to the first transistor and the second transistor to counter any change that occurs in the input signal appearing at the input terminal.

22. (Previously presented) The buffer circuit of claim 2 wherein the first transistor and the second transistor are balanced when a change occurs in the input signal appearing at the input terminal.

23. (Previously presented) The buffer circuit of claim 7 wherein the first transistor and the second transistor are balanced when a change occurs in the input signal appearing at the input terminal.

24. (Previously presented) The buffer circuit of claim 9 wherein the first transistor and the second transistor are balanced when a change occurs in the input signal appearing at the input terminal.

25. (Previously presented) The buffer circuit of claim 10 wherein the first transistor and the second transistor are balanced when a change occurs in the input signal appearing at the input terminal.